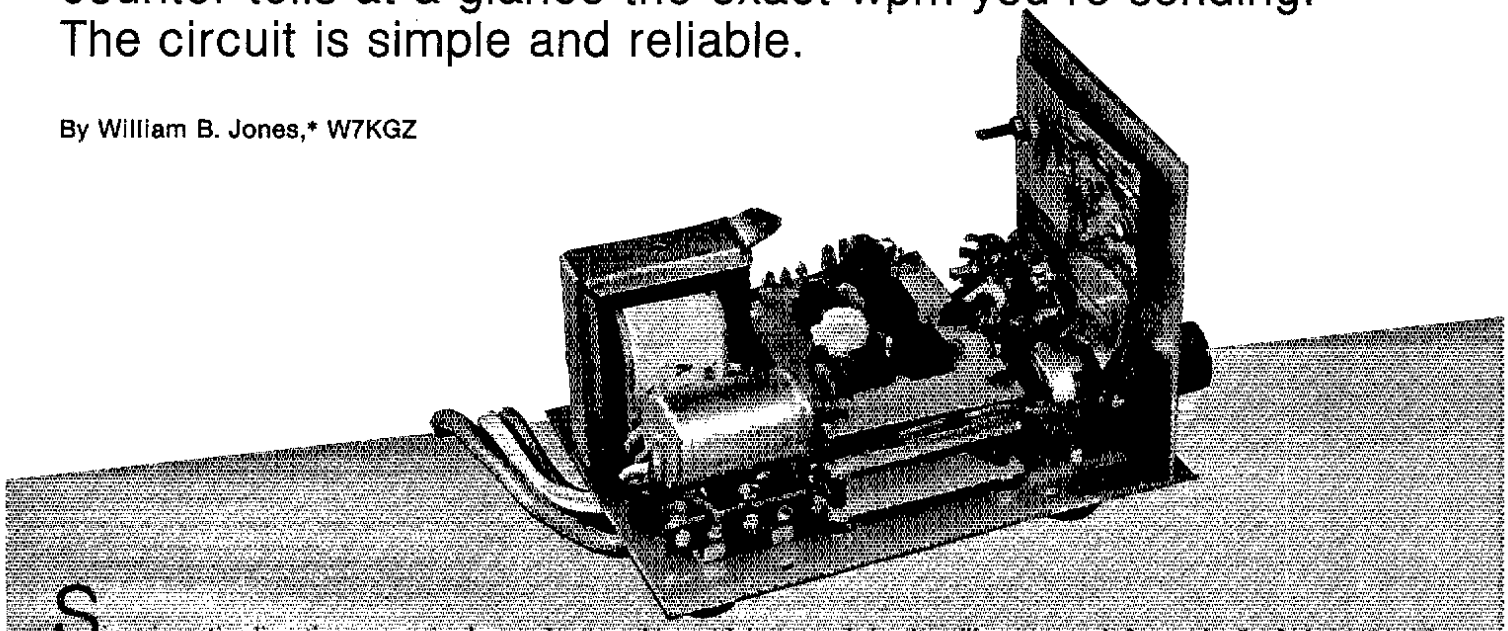
A Digital Speed Readout for the Electronic Keyer

Say good-bye to guessing code speeds. This nifty digital counter tells at a glance the exact wpm you're sending. The circuit is simple and reliable.

By William B. Jones,* W7KGZ



Since incentive licensing was revived a few years ago, many amateurs have been working to upgrade their tickets. Upgrading often means another code test. Another code test means lots of practice at the correct speed if you are to get a shot at the written part of the exam. Until now determining the speed of transmitted code has been mainly a matter of guesswork. But with this simple digital speed readout for an electronic keyer, the guesswork can be cast aside; with a glance you know the precise speed at which characters are formed.

What's Inside Counts

Converting clock pulses of a keyer into a numerical display is a very simple process. *The Radio Amateur's Handbook* tells us that most modern electronic keyers use a clock circuit which feeds a flip-flop dot generator and the code speed in wpm can be determined directly from the formula: wpm = 1.2 × clock frequency (Hz). To put it another way, if we count the number of clock pulses in exactly 1.2 seconds, the readouts will show the code speed directly in words per minute.

The schematic diagram in Fig. 1 clearly indicates the simplicity of the system. The three IC's (7490, 7475 and 7447) associated with the DL-747 readouts perform the necessary counting, storage and decoding functions. The series of articles in *QST*

*32104 N.E. 76th St., Vancouver, WA 98662

References appear on page 13.

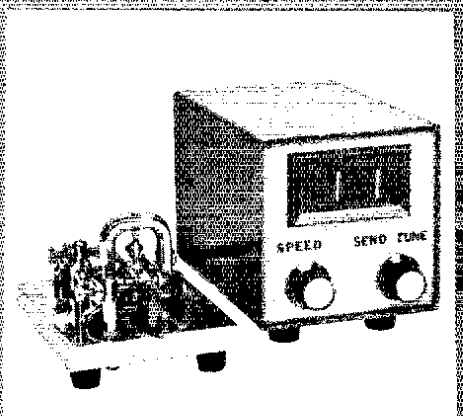
about working with integrated circuits will give the reader an understanding of how this part of the circuit works.

The three remaining ICs establish the 1.2-second time base as well as generate the latch and reset pulses necessary to update the readouts. The 555 timer (U9) is wired as an astable multivibrator. The time interval between each negative-going transition is set by means of the 100-kΩ potentiometer calibration control. More about this later.

Latch and reset pulses are derived from the 7474 edge-triggered D-type flip-flop. This part of the circuit is taken from the *TTL Cookbook*.[2] As the 555 switches from a logic one to a logic zero, a pulse is generated from pin 5 of the 7474. The pulse is differentiated and fed to one section of the 7400 quad NAND gate. The NAND gate inverts the pulse which is then fed to the 7475 quad latches. Bringing the 7475 enable lines from low to high allows the display to update.

Reset pulses are derived the same way as the latch pulses except that now the low-to-high transition from the 555 is used to generate an output from the $\overline{Q}$ pin of the 7474. Again, the pulse is differentiated, inverted and fed to the zero-reset inputs of the 7490 decade counter. This system is simple and most reliable.

If you have followed the logic to this point, then the need for a continuous series of pulses to count should seem obvious. Some electronic keyers use a keyed clock; in other words the clock is only running while a character is being generated. The keyer used with the prototype digital speed readout performed this way but an alternative was to construct a copy of the keyer clock and wire it so that it ran continuously. The output from *this* clock is actually the one being counted. To arrange for the two clocks to run at the same speed, identical timing components are used and the speed control is a dual pot with identical values and tapers. Naturally, the accuracy of the readout is dependent upon the matching of the speed-control components. Tantalum capacitors and quality potentiometers are recommended. Tracking



The W7KGZ digital readout code speed counter that provides a positive check on the speed of character formation. This compact unit has instant eye appeal.

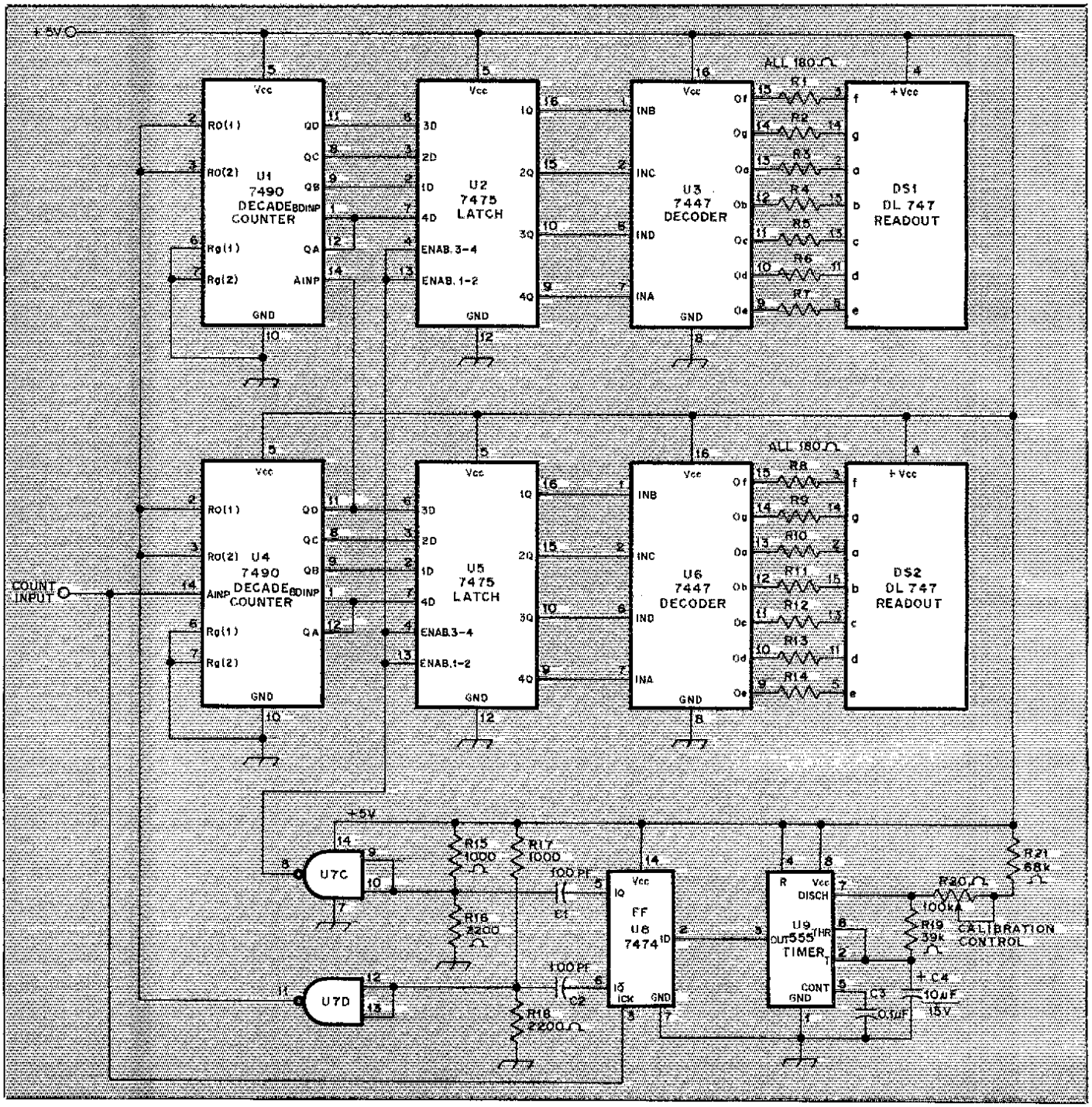


Fig. 1 — Schematic diagram for the digital speed readout. The three ICs associated with each DL-747 LED perform the counting, storage and decoding functions. Resistance values are in ohms and all fixed resistors are 1/4 watt. R1-R14, incl., are 180 ohms. R20 is a 100-kΩ miniature linear-taper potentiometer. The 555 is wired as an astable multivibrator. No connections are made to IC pin numbers not shown. Capacitors with polarity indicated are electrolytic.

DS1, DS2 — Seven-segment common anode LED digital display readout, Litronix type DL-747 or equiv.
U1, U4 — TTL decade counter, type 7490.
U2, U5 — TTL 4-bit bistable latch, type 7475.
U3, U6 — TTL BCD to seven-segment decoder/driver, type 7447.
U7 — TTL quadruple 2-input positive NAND gate, type 7400; two sections unused.
U8 — TTL dual D-type positive edge-triggered flip-flop with preset and clear, type 7474.
U9 — Timer IC, 555.

was within one word per minute throughout the entire speed range on the prototype. The readout has since been adapted for use with the author's keyboard keyer which has a continuously running clock. Of course it was not necessary to build a duplicate clock in that case.

In the version shown in the photograph, the actual keyer is built into the same case as the digital display. The keyer was described in *QST* for January, 1975.[3] It is a superb performer, the third in a series built by the author. All worked perfectly upon initial testing.

Perfboard construction was used throughout as a means of saving time and also for the sake of neatness. Because troubleshooting a defective IC can be difficult, the installation of IC sockets in the circuit seems well worth the small investment. Teflon insulated wire interconnects the various pins of the sockets and other components.

The prototype was constructed on three separate pieces of perfboard cut to the same size for stacking. The keyer was built

first. After testing, it was set aside while assembly of the display part of the project took place. The third board contains the 555 timer, 7474 flip-flop and the 7400 gates. After each module had peformed properly, they were all stacked, using long machine screws and metal spacers or nuts to hold the boards in position. Small loops of tinned no. 16 wire inserted in the perfboard serve as terminal connections. Common connections for each board, such as ground and Vcc, are positioned directly over each other in order to provide the shortest possible connection. Although not shown in the schematic diagram, each module has a 0.01-μF disk ceramic capacitor connected directly between the ground bus and the +5-volt supply line. In addition, the cable to the paddles and the power supply wires are similarly bypassed to prevent rf from entering the cabinet.

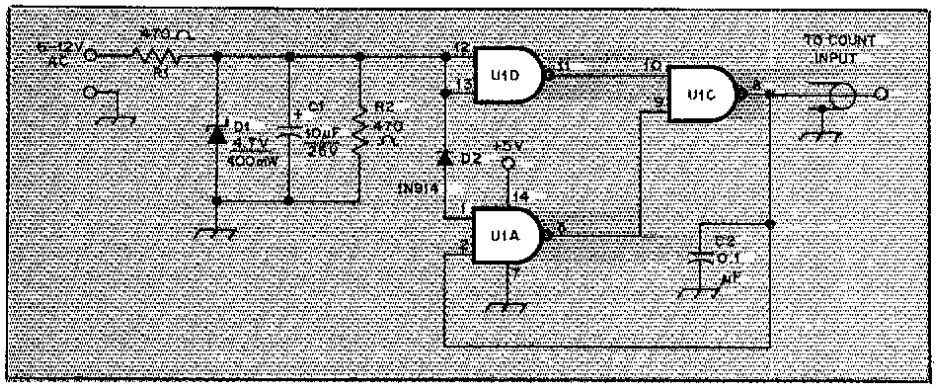


Fig. 2 — This circuit provides a means of obtaining a calibration signal for the digital speed readout unit. It squares the sine wave from the 60-Hz ac line, clipping the negative part and is therefore TTL compatible.

D1 — Zener diode, 4.7 V, 400 mW, 1N750 or equiv.
D2 — Silicon diode, 1N914 or equiv.
R1, R2 — 470 ohm, 1/4-watt resistors.
U1 — TTL quadruple 2-input positive NAND gate, type 7400; one section unused.

Calibration

After all the boards are interconnected and working correctly, calibrating the unit is the next task. Probably the simplest and most accurate method of calibration is to sample the 60-hertz line frequency. The circuit of Fig. 2 is taken from Calectro's *Digital Handbook.*[4] It serves to square the sine wave and clip the negative part in order to assure TTL compatibility. With the "count input" lead of the display temporarily connected to the output of the calibrator, the 100-kΩ calibration control is adjusted for a reading of 72 on the readouts. This corresponds to exactly 1.2 seconds for the time base. The calibrator can be made a permanent part of the unit if so desired. The 555 is quite stable over long periods of time although recalibration can be accomplished every few months for the sake of the purist. An spdt toggle switch can be used to connect either the calibrator or keyer to the readout.

The digital speed readout has been in use at W7KGZ for many months, becoming a most valuable addition to the station. When sending at the higher speeds, as with a keyboard keyer, there is reassurance in knowing exactly at what speed the characters are being formed. Progress in code speed can be measured directly in wpm and when the guy on the other end of a QSO says he can copy 40, you can find out for sure! QST

References

[1]Hall and Watts, "Learning to Work with Integrated Circuits," *QST* for January through July and November, 1976, and June, 1977. The series has also been published in booklet form (ARRL Publication no. 32) and is available for $2 per copy (in USA) from ARRL Headquarters, 225 Main St., Newington, CT 06111.

[2]Lancaster, *TTL Cookbook,* First Edition, Howard W. Sams and Co., Inc. 1974, p. 212.

[3]Fox, "An Integrated Keyer/TR Switch," *QST* for January, 1975.

[4]*Digital Handbook*, Catalog no. FR 169, G. C. Electronics, 400 S. Wyman St., Rockford, IL 61101.

Feedback

☐ The feedback information which appeared on page 85 of May 1978 *QST* shows the solid black etching pattern for the 20-Meter High-Performance Direct-Conversion Receiver (Rusgrove, April 1978 *QST*, page 11) inverted from the way it should appear. The shaded pattern with the parts information overprinted in orange is correctly shown from the *foil* side of the board. No big problem if you make a transparency for exposing a circuit board, though. Simply invert the transparency before making the board exposure.

☐ Are you duplicating the DoppleScAnt (Rogers, page 24 of May 1978 *QST*)? If so, you should know that a number of errors appear in the schematic diagram, Fig. 4. The nature of the errors makes it difficult to describe corrections adequately in words, and limited space prevents us from republishing the diagram in *QST*. A corrected schematic is available upon request (no charge) from ARRL, Dept. TDSC, 225 Main St., Newington, CT 06111. A stamped return envelope will expedite the handling. The corrected diagram contains component numbers, required if you're working with the etching templates. (We'll be including the corrected diagram with future template orders.) See the footnote on page 28 of May *QST* regarding template availability.

☐ In "An Audio Continuity Tester" (May 1978 *QST*, page 21), author K1TX advises that the transistor shown in Fig. 1 should be diagramed as shown below.

☐ In the "Modular Control Unit — Just for Repeaters" (Shriner, May 1978 *QST*, page 11), the presentation of the etching patterns in Fig. 3 requires clarification. The board is *double-sided;* each pattern correctly shows the foil. Components are mounted on the side with the lettering, REPEATER CONTROL.

Parts placement guide for the Audio Continuity Tester with corrected transistor-basing diagram.