by Graham Moore G4DML

Bug Key With 528-Bit Memory

Many radio amateurs are either interested or have participated in communication on the v.h.f. bands using meteor scatter (m.s.). Although it is possible to make contact using s.s.b. via m.s. this usually results in a sore throat and a very warm tape recorder before a successful contact is made. High speed c.w. offers a much more reliable way of communicating under these circumstances, this being due to the proportionally smaller bandwidth required and hence the much improved signal to noise ratio.

This article describes a Morse keyer with an integral memory that will replay any Morse that is input at any selected speed. Thus with a 3-speed tape recorder you will be able to communicate at, say, 400 letters per minute (approximately 80 w.p.m.), even if you can only send and receive at 20 w.p.m.

Circuit Description

The keyer consists of a standard "el-bug" circuit around IC3, gated to both the keying relay, RLA, and to the recirculating shift register memory. This is made up of eight 4031 64-stage static shift registers, designed so that the data once entered shifts continuously around the loop formed by these i.c.s and their associated circuitry.

Both keyer and memory are clocked by the continuously variable c.m.o.s. oscillator formed by IC1. The clock drive to the shift register can be disabled so that the keyer can be used as a standard el-bug without storage. This method of storing the data was chosen as it alleviates the problem of generating the address encoding and decoding that would be required if RAM type memory was used.

The data is read in purely as a serial data stream and read out in exactly the same way; note however that the data is stored inverted in order to simplify start and stop bit identification. In order to locate the start of the message a synchronising pulse of eight blanks is left at the beginning of any data entry. The circuitry that detects this pulse, IC8 and IC10, is also used at the other end of the memory, IC9 and IC11, to enable any large blanks in the stored message to be run through at very high speed. This is done by automatically switching oscillator speeds by IC2 and IC7 when more than eight blanks are detected by IC9 and IC11. When the first data bit is detected by IC8 and IC10 the clock is switched back to normal speed and keying continues.

The recirculating shift register format is also convenient if only a small memory is required. Thus if only 128 bits of storage are required only two of the 4031 devices need be inserted and the output pin (pin 6) bridged to TP1.

The complete keyer is constructed using c.m.o.s. logic to enable it to be used for long periods on NiCad batteries. A sidetone is included on the keyer p.c.b. but as most transceivers nowadays have integral sidetone a switch is fitted on the keyer to disable the tone. A socket is fitted on the rear of the keyer for an external 12 volt d.c. charging/operating supply.

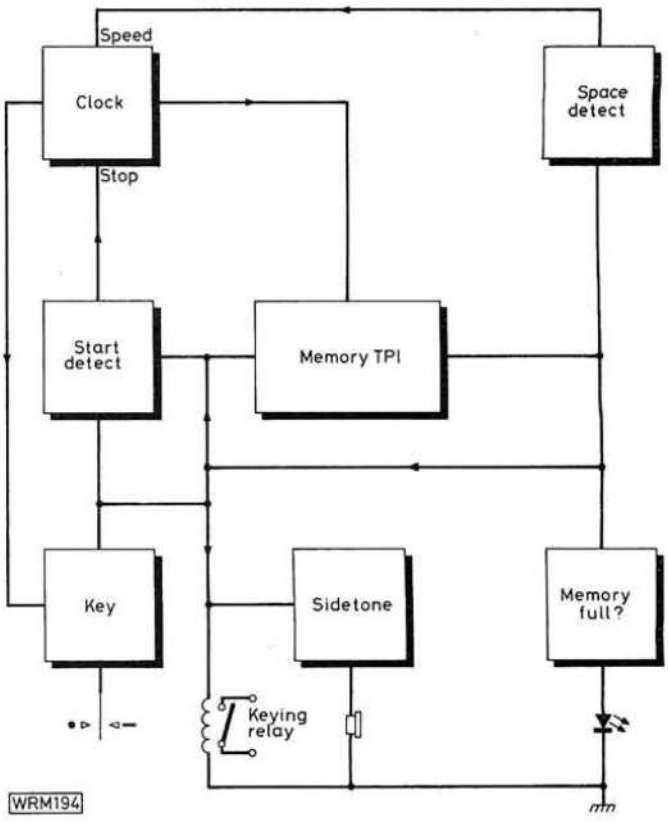


Fig. 1: Block diagram of the Memory Keyer

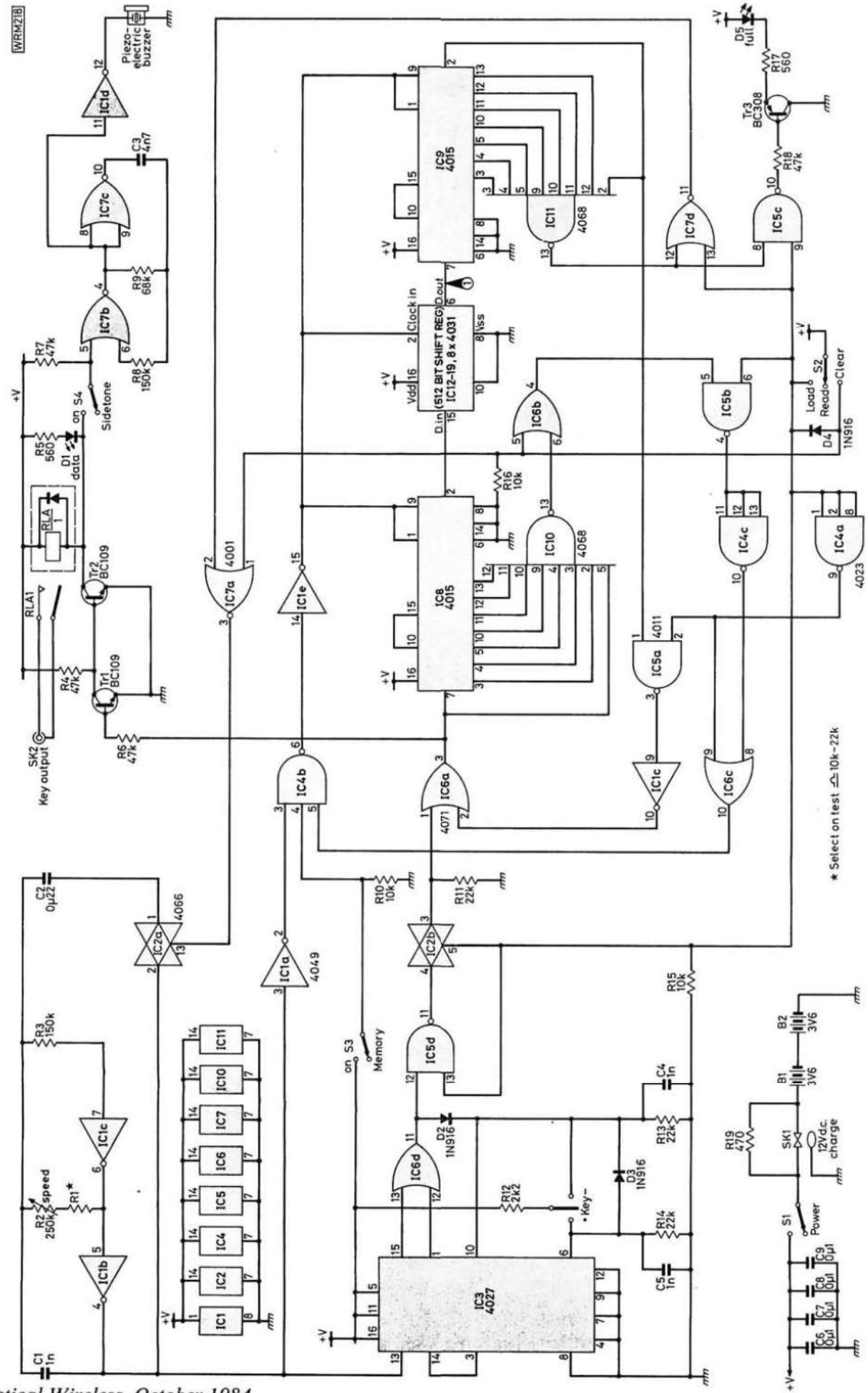
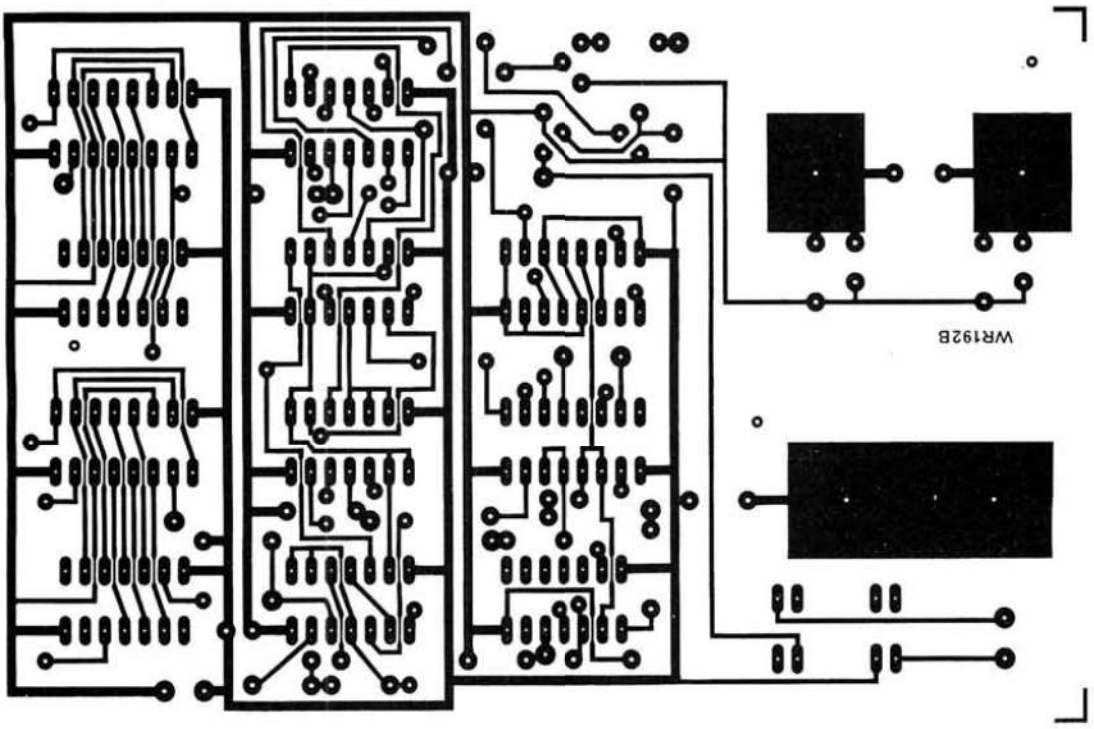


Fig. 2: Circuit diagram of the 528-bit Memory Keyer



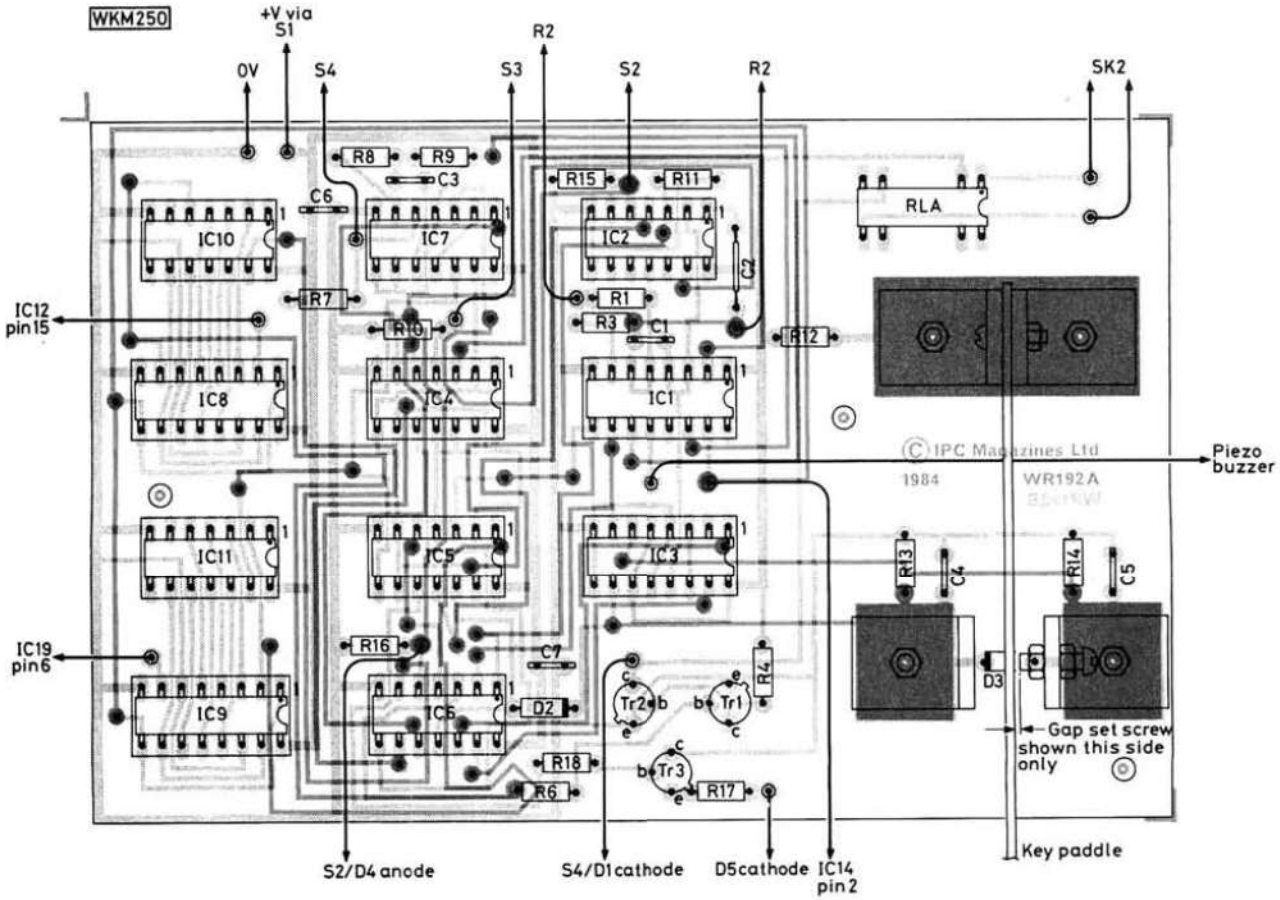
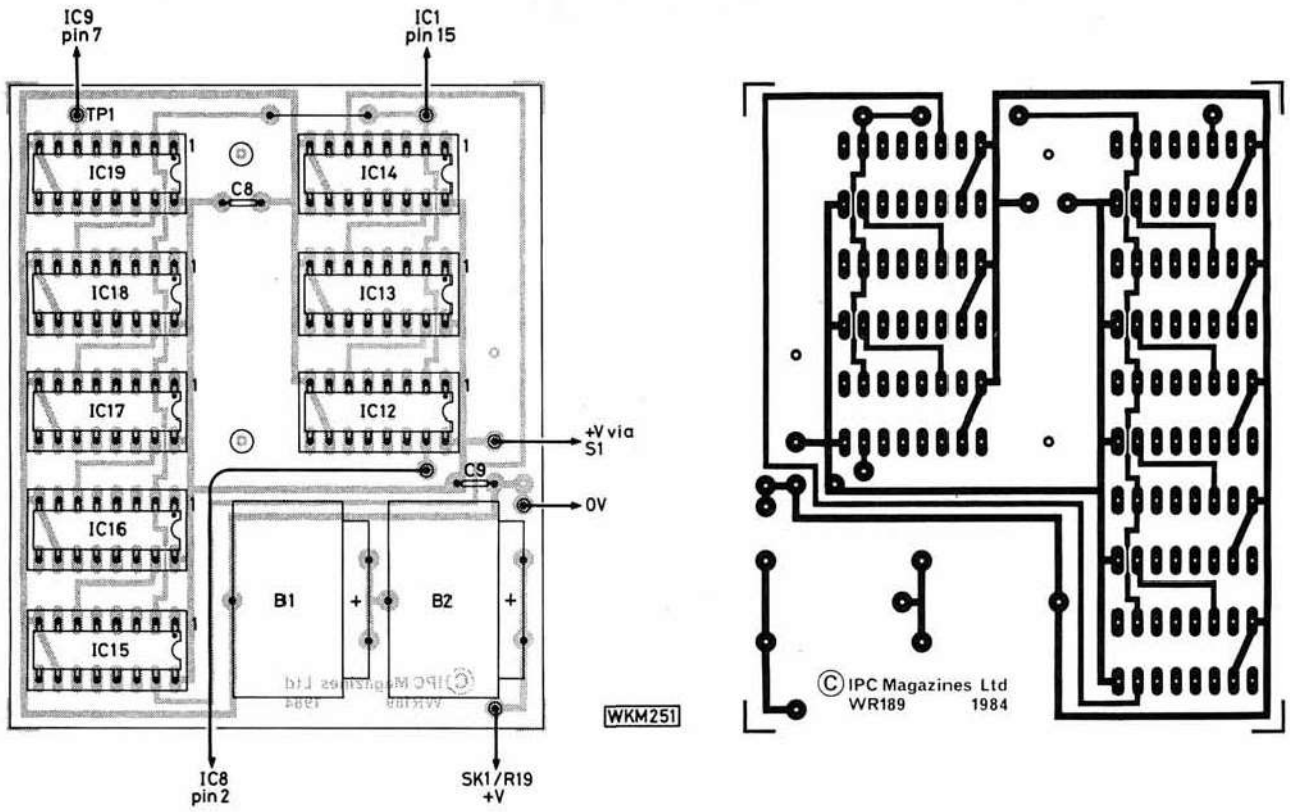


Fig. 3: Full size p.c.b. track pattern (lower non-component side) and component placement diagram of the double-sided control board. Ensure all through-board links are soldered to the pads provided, taking particular care with those located underneath i.c. sockets which are virtually impossible to check once the sockets are installed



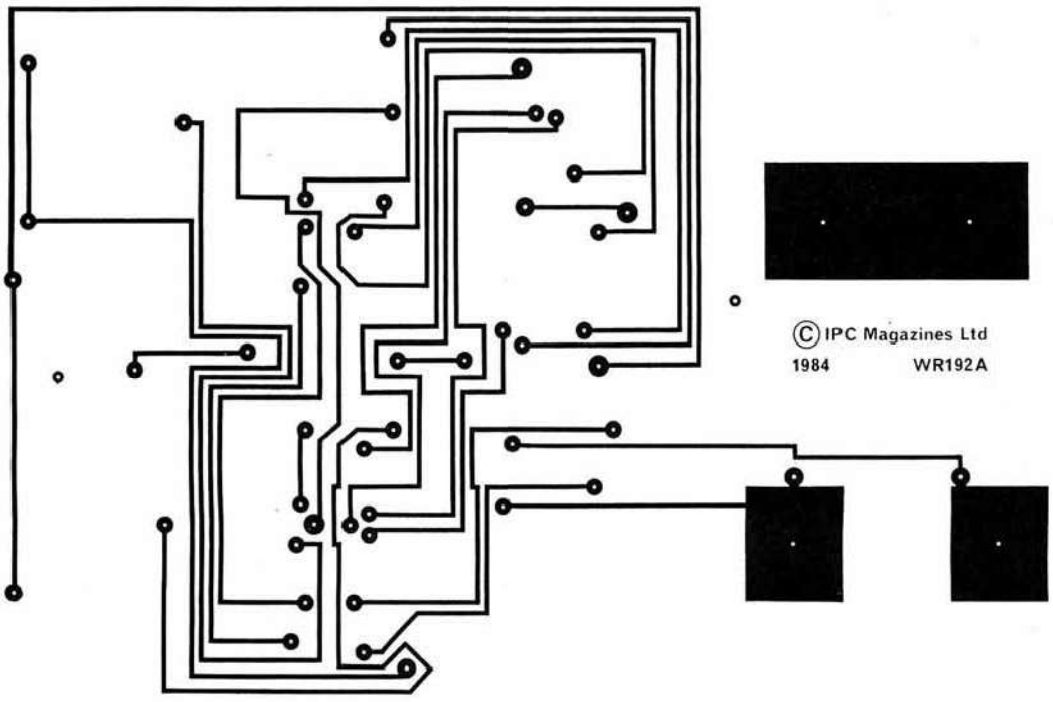


Fig. 4: (Top) Full size p.c.b. track pattern and component placement diagram of the single-sided memory board. (Below) The upper (component side) track pattern of the control board

Functional Description

MEMORY ON/OFF: This enables the clock to the re-circulating memory. When in the OFF position the keyer can be used as a normal el-bug with no storage facility.

LOAD: When used in conjunction with MEMORY ON, any keyed data is loaded into the memory. The clock is automatically disabled when no keying is present so as not to run through the memory filling it with blanks. Note that this switch must be in the LOAD position to enable the paddle to operate the keyer.

CLEAR: When used in conjunction with MEMORY ON the entire memory space is cleared in approximately two seconds. It must be pressed and held down until the memory FULL l.e.d. extinguishes at the start of every load cycle.

READ: In this position with the memory switched ON, information stored in the memory will be read out to the keying relay and DATA l.e.d.

DATA and FULL l.e.d.s: These two indicators are included on the keyer so that an eye can be kept on the operation of the unit.
The DATA l.e.d. indicates the information being sent to the keying relay.
The FULL l.e.d. indicates when there are eight more empty memory locations left. Normally unless the data entry can be completed in this time, the memory will then have to be cleared and a shorter message input.

The SPEED control is self-explanatory, allowing data to be keyed in at one speed and output at another. A rate of 400 letters per minute is the normal speed used for m.s. contacts.

BUYING GUIDE

Most components used in this project are readily available through stockists advertising in *Practical Wireless.* The d.i.l. relay is available from Cirkit stock No 46–61500 or alternatively RS 349–383. The c.m.o.s. 4031 i.c. is stocked by Maplin Electronics.

Approximate Cost £40

Construction Rating Intermediate

★components

Resistors

¼W 5% Carbon film

560Ω	2	R5,17
2·2kΩ	1	R12
10kΩ	3	R10,15,16
22kΩ	3	R11,13,14
47kΩ	4	R4,6,7,18
68kΩ	1	R9
150kΩ	2	R3,8

1W 5% Carbon film

470Ω	1	R19

Potentiometers

¼ inch spindle, ½W carbon track

250kΩ	1	R2

Capacitors

Ceramic

1nF	3	C1,4,5
4·7nF	1	C3
0·1µF	4	C6–9
0·22µF	1	C2

Semiconductors

Diodes

1N916	3	D2,3,4
Red l.e.d.	2	D1,5

Transistors

BC109	2	Tr1,2
BC308	1	Tr3

Integrated circuits

4001	1	IC7
4011	1	IC5
4015	2	IC8,9
4023	1	IC4
4027	1	IC3
4031	8	IC12–19
4049	1	IC1
4066	1	IC2
4068	2	IC10,11
4071	1	IC6

Miscellaneous

Switched 3·5mm jack (1); phono socket (1); 5V d.i.l. reed relay (1); 3·6V, 100mAh p.c.b. mounting NiCads (2); Miniature s.p.s.t. toggle switch, S1,3,4; s.p.d.t. centre-off, one side biased (RS 317-112) S2; 155 x 115 x 65mm case (Cirkit DX1); 16 pin d.i.l. sockets (12); 14 pin d.i.l. sockets (7); Piezo buzzer PB2720; p.c.b.'s (2); Veropins; paddle materials; control knob; nylon stand-off pillars (6).

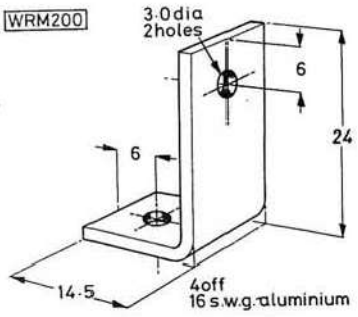
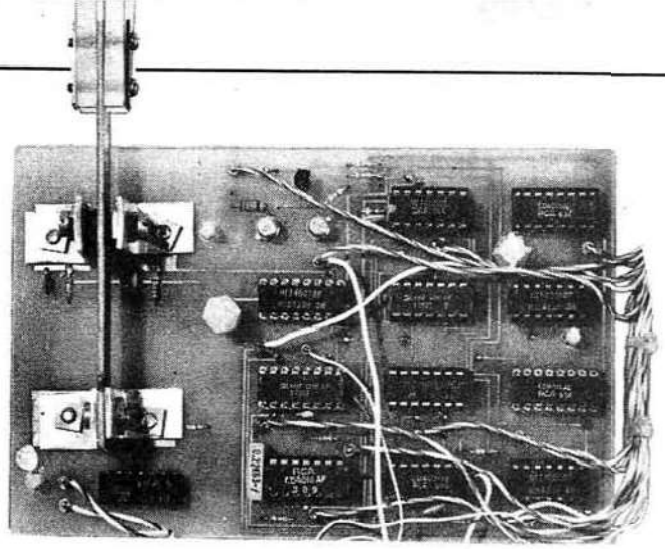
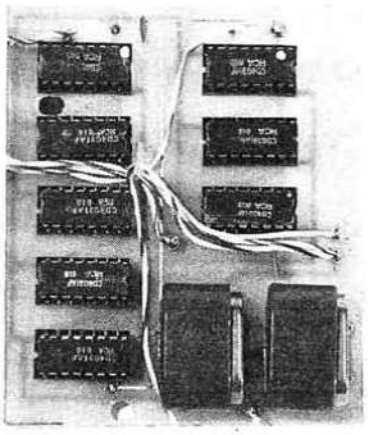


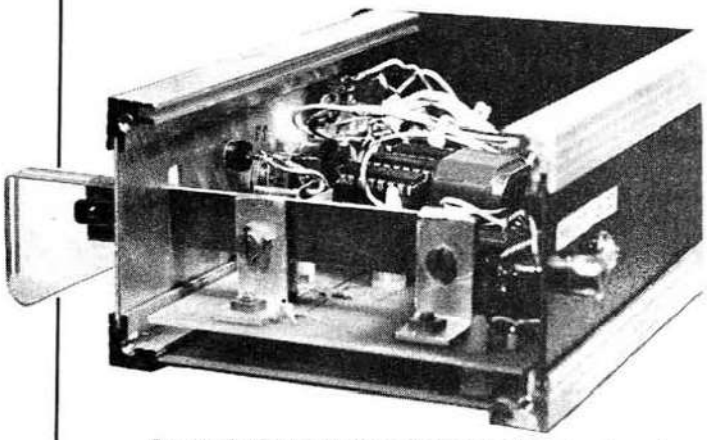
Fig. 5: Details of the four bug key mounting brackets



The author's prototype control board



The memory board together with 7·2V NiCad supply



An end view of the prototype keyer showing the bug key. The movable wiper is formed from a 100 × 12mm piece of 1·5mm double-sided p.c.b.

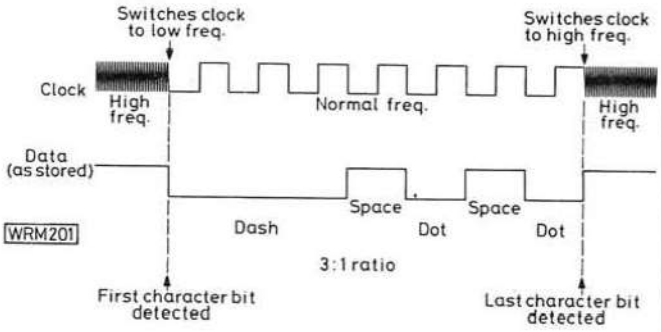


Fig. 6: The timing diagram

Construction

No special instructions are necessary other than the usual warning about handling c.m.o.s. devices. Even though most of these are now statically protected it is still not advisable to shuffle across a synthetic carpet on the way to the workbench!

Make sure all through holes are soldered on both sides of the board including those under the i.c. sockets. The "select on test" resistor R6 is to enable any range of speeds to be selected—22kΩ being the nominal value.

Testing the Keyer

After constructing the unit and confirming that there are no shorts or dryjoints, check that each NiCad battery measures between 3 and 3·9 volts.

Switch on and leave the memory switched OFF. Using either an oscilloscope or a logic probe, confirm that a squarewave clock is present on both IC3 pin 13 and IC4 pin 3. Ensure that this clock varies in frequency as the SPEED control is turned. Connect the same probe to pin 2 of any 4031 device on the memory p.c.b. Switch the memory ON and confirm that the clock now is present at this pin.

Next switch to LOAD and turn the memory OFF. Confirm that as the paddle is moved the keying relay and sidetone operate. Switch the memory ON and depress CLEAR for about two seconds—the FULL l.e.d. should extinguish. Now switch to LOAD and key in some data and then switch to READ and confirm that the keyer repeats faithfully the data that was input, at any speed set by the SPEED control.

Once again CLEAR the memory and with the speed set to maximum hold the paddle so that a continuous stream of dots is loaded into the memory. After approximately 15 seconds the FULL l.e.d. should illuminate indicating that there is no more memory available.

Conclusion

The prototype of this keyer was built a while ago and has been in constant use since. Several dozen m.s. contacts have been made and once operating the keyer has been mastered it should perform for many hours on a single recharge. Several more of these keyers have been built and all have worked first time with not a single problem. Happy QSOing and Gd DX. ●